## ABSTRACT

A phase control loop circuit for tuning to a reference frequency signal having a phase lock loop (PLL) circuit being responsive to a reference frequency signal having a reference frequency, said PLL circuit including a voltage control oscillator (VCO) for generating a VCO output, said PLL circuit for generating a PLL output, said phase control loop circuit processing said VCO output to generate an output frequency signal having an output frequency, in accordance with an embodiment of the present invention. The phase control loop circuit further includes a coarse tuning circuit being coupled to said PLL circuit, said coarse tuning circuit being responsive to said PLL output for processing the same to generate a counter output, said VCO being responsive to said counter output, said counter output for coarse tuning said output frequency signal to said reference frequency signal, said coarse tuning circuit further responsive to a lock detection (LD) signal, said LD signal for controlling said counter output to cause said output frequency to be within a predetermined range of frequencies including said reference frequency, said PLL circuit for fine tuning said output frequency signal to said reference frequency signal, wherein said PLL circuit and said coarse tuning circuit tune the output frequency to a reference frequency included in a wide range of frequencies.